Hardware/Software Co-Verification is a methodology that enables the execution of Embedded System Software on a simulated representation (Virtual Prototype) of the System Hardware.
Over 120 Processor Models

ARM7, ARM9
ARM10, ARM11

C55X, C64X

Oak, Teak, TeakLite, Palm

4K, 4KE, 5K, 20K

PowerPC 40x, 44x

PowerPC 603, 74x, 75x, 8XXX
PowerQUICC I, II, III

SH1-SH4, SH-DSP

Xtensa

ZSP

RM7000

Models also available for ARC, NEC, Toshiba, Mitsubishi, Matsushita, Fujitsu, Philips, Samsung, Faraday, Trimedia, Lucent, ETRI, Analog Devices, Intel, StarCore, and Others
Seamless Version 5 Performance Profiler

Software Profile

Arbitration Delay

CPU

Cache

Memory

Bus Master
Verisity Specman Elite Integration Extends the Verification Possibilities

- Extend the HW/ SW interaction verification through Specman/ Seamless Integration:
  - Input generation
  - Checking correct HW/ SW interaction
  - Functional coverage of HW & SW
Seamless with C-Bridge

- Single Solution for C, C/RTL and RTL based Co-Verification
  - All Seamless PSPs support C-Bridge Functionality (including ARM, PowerPC, MIPS, TMS320, etc.)
- Connect C HW functionality to processor bus
  - Support for multiple dialects of C through API/DLL
    - ANSI C, C++, SystemC
  - Enables C-based prototyping and accelerated verification
Seamless with C-Bridge

Seamless Connects ISS/Debuggers to Bus Interface Models in RTL

The Internal/External Memories Link to the Seamless Memory Server

C Module Links to Seamless through C-Bridge API as DLLs

Optional Connections: PIM & Host Code Debugger
Iterative “Spec-to-RTL” Flow

- **System Optimization**
  - System Performance data
  - System Optimization

- **Co-verification**
  - Functional correctness
  - Verification ready design

- **Integration**
  - Architectural refinement
  - Integration

- **System Assembly**
  - Hardware Accelerators
  - Platform, Bus-based IP, Algorithms
  - System Assembly

- **Perf Analysis**
  - Swr → Hwr
  - Block-level optimization
Single Kernel, Language-Neutral

- #1 in Mixed-Simulation Market
  - Single Kernel
  - Same GUI & Commands Regardless of Language
  - All Debug Capabilities Apply to Verilog, VHDL, & SystemC
  - Easy Upgrade from 1 Language to Include Another (No New Tools/Features to Learn)
  - Support Simultaneous PLI & FLI Access
- True Mixed-Language Solution
Optimized Native Compilation

- Compile HDL Directly to Executable
  - No Intermediate Compilations Required
  - Fastest Compilation Time

- Platform-Independent
  - Compile on One Platform, Simulate on Another
  - Executable Optimized for Host Machine When Invoked
  - Best Performance
ModelSim 5.8 = Hub of Verification

- Complete Verilog 2001, SystemVerilog, VHDL 2002
- Native C/C++ & SystemC Support
- Single Kernel, Trilingual Simulator
- Built-in Assertion Engine
- PSL Support
- Condition, Expression, Enhanced Toggle Coverage
- Improved Performance
- More Debug Capabilities